as the present application, and to that extent are arguably related to the present application, are incorporated herein by reference.

Please replace the paragraph at Column 4, line 35 with the following:
Please replace the paragraphs beginning at Column 4, line 66 and ending at Column 6, line 2 with the following:

Referring once more to FIG. 1a, during power-up in a periphery stress test mode, Control' bar derivative signal 23 (shown at Node [3] 4 of FIG. 1) and Control' derivative signal 27 (shown at Node [4] 3 of FIG. 1) are both a low logic state and signal 21 at Node 5 is forced to a high logic state. This gives the appearance that Clock input signal 12 was a low logic state. Conversely, when Control' bar derivative signal 23 and Control' derivative signal 27 go to high logic states, signal 21 is forced to a low logic state which gives the appearance that Clock signal 12 was a high logic state. Thus, a high logic state on controls signals Control' bar derivative signal 23 and Control' derivative signal 27 during a periphery stress test mode forces the equivalent of a high going clock input. During a memory cell stress test mode, the equivalent of a low going clock input is forced. Upon power-up of the device, Power-On-Reset signal 16 goes high and Clock derivative signal [12] 38 is forced to a low logic state during which the master latch of the device is loaded with data and allowed to conduct. Following completion of the power-on reset cycle, Power-On-Reset signal 16 does low and data is latched into the master latch; also data is loaded into the slave latch [which is allowed to device conduct]. Using the circuitry of FIG. 1a, the state of Clock derivative signal [12] 38 is forced to the desired logic state during a test mode, either a periphery stress test mode or a memory cell stress test mode.

In the Claims:

Please amend claims 18-19, 22-27, 31-35, and 38-39 per below (all the claims 18-39 added in the reissue application are included for the convenience of the examiner).

18. A method, comprising:
providing power to an integrated circuit;

loading a first data bit into a master latch before the power attains a predetermined level, the master latch being disposed on the integrated circuit;

generating a second data bit from the first data bit;

latching the first data bit in the master latch; and

loading the second data bit into a slave latch that is disposed on the integrated circuit.

19. The method of claim 18, further comprising causing the integrated circuit to enter a test mode before the power attains the predetermined level.

20. The method of claim 18 wherein generating the second data bit comprises generating the second data bit equal to the first data bit.

21. The method of claim 18 wherein generating the second data bit comprises generating the second data bit equal to a complement of the first data bit.

22. The method of claim 18 wherein generating the second data bit comprises generating the second data bit before and after the power attains the predetermined level.

23. The method of claim 18 wherein:

loading the first data bit into the master latch comprises simulating an external clock signal having a first clock state; and

latching the first data bit in the master latch and loading the second data bit into the slave latch comprise simulating the external clock signal having a second clock state.

24. The method of claim 18 wherein:

loading the first data bit into the master latch comprises simulating an external clock signal inside the integrated circuit, the clock signal having a first clock state; and

latching the first data bit in the master latch and loading the second data bit into the slave latch comprise simulating the clock signal having a second clock state.

25. A method, comprising:

generating a power-on reset signal having a first reset state when power supplied to an integrated circuit has a predetermined first level;

generating the power-on reset signal having a second reset state when the power has a second predetermined level;

loading a first data bit into a master latch of the integrated circuit in response to the power-on reset signal having the first state;

generating a second data bit from the first data bit;

storing the first data bit in the master latch in response to the power-on reset signal having the second state; and

loading the second data bit into a slave latch of the integrated circuit in response to the power-on reset signal having the second state.

26. The method of claim 25 wherein:

generating the power-on reset signal having the first state comprises generating the power-on reset signal having the first state when an integrated-circuit supply voltage has a first predetermined voltage level; and

generating the power-on reset signal having the second state comprises generating the power-on reset signal having the second state when the supply voltage has a second predetermined voltage level.

27. The method of claim 25, further comprising causing the integrated circuit to enter a test mode when the power has the first predetermined level.

28. The method of claim 25 wherein generating the second data bit comprises generating the second data bit in response to the power-on reset signal having either the first state or the second state.

29. The method of claim 25 wherein storing the first data bit in the master latch and loading the second data bit into the slave latch comprise generating a test signal having a first test state.

30. The method of claim 25 wherein storing the first data bit in the master latch and loading the second data bit into the slave latch comprise generating multiple test signals each having a first test state.

31. The method of claim 25 wherein storing the first data bit in the master latch and loading the second data bit into the slave latch comprise:
generating a test signal having a test state; and
simulating an external clock signal having a clock state in response to the test signal having the test state.

32. The method of claim 25 wherein:
loading the first data bit into the master latch comprises simulating an external clock signal having a first clock state in response to the power-on reset signal having the first reset state; and
storing the first data bit in the master latch and loading the second data bit into the slave latch comprise,
generating a test signal having a test state, and
simulating the clock signal having a second clock state in response to the test signal having the test state.

33. The method of claim 25 wherein:
loading the first data bit into the master latch comprises,
simulating an external clock signal having a first clock state in response to the power-on reset signal having the first reset state,
generating a test signal having a test state, and
generating the first data bit in response to the test signal; and
storing the first data bit in the master latch and loading the second data bit into the slave latch comprise simulating the clock signal having a second clock state in response to the power-on reset signal having the second reset state and the test signal having the test state.

34. The method of claim 25 wherein:
loading the first data bit into the master latch comprises,

simulating an external clock signal having a first clock state in response to the power-on reset signal having the first reset state,

generating a test signal having a first test state, and

generating the first data bit in response to the test signal; and

storing the first data bit in the master latch and loading the second data bit into the slave latch comprise,

generating the test signal having a second test state, and

simulating the clock signal having a second clock state in response to the power-on reset signal having the second reset state and the test signal having the second test state.

35. A method, comprising:

providing power to an integrated circuit;

loading a first data bit into a master latch before the power attains a predetermined level, the master latch being disposed on the integrated circuit;

latching the first data bit in the master latch; and

loading the first data bit into a slave latch of the integrated circuit.

36. The method of claim 35 wherein:

loading the first data bit into the master latch comprises generating a clock signal having a first clock state; and

latching the first data bit in the master latch and loading the first data bit into the slave latch comprise generating the clock signal having a second clock state.

37. The method of claim 35 wherein:

loading the first data bit into the master latch comprises generating a clock signal inside the integrated circuit, the clock signal having a first clock state; and

latching the first data bit in the master latch and loading the first data bit into the slave latch comprise generating the clock signal having a second clock state.

38. The method of claim 18 wherein:

latching the first data bit comprises latching the first data bit in the master latch after powering up the integrated circuit; and